## REMARKS

Applicant wishes to thank the Examiner for the attention accorded to the instant application, and respectfully requests reconsideration of the application as amended.

### Formal Matters

Claims 11-26 are the claims currently pending in the Application. Claims 11 and 16 are amended herein. Specifically the limitations of sequentially reading, and determining whether the source code is to be modified, are moved from claim 16 to claim 11. No new matter has been added.

### Rejection of Claims 11-15 and 17-19 Under 35 U.S.C. §103

Claims 11-15 and 17-19 are rejected under 35 U.S.C. § 103(a) as unpatentable over Tammemae et al., "AKKA: A tool for cosynthesis and prototyping", The Institute of Electrical Engineers, UK, 1996 (hereinafter "Tammemae") in view of Chang et al., U.S. Patent No. 6,269,467 (hereinafter "Chang"). This rejection should be withdrawn based on the comments and remarks herein.

The present application provides an inventive method for performing a performance evaluation of at least one bus at a high-level stage of the computer architecture design and development process. The bus is part of source code structured to represent hardware and software units; the bus realizes the data traffic between the hardware and software units. The evaluation process includes creating an evaluation function for counting data traffic that occurs on one bus, analyzing syntax, modifying at least one element of the source code based on the evaluation function, and performing the performance evaluation by simulating source code elements and counting the data traffic on the bus. Thus the present invention simulates hardware and software to evaluate proposed hardware and software configurations.

The Examiner states that Tammemae and Chang do not expressly teach sequentially reading in the source code line by line while effecting syntax analysis, and also do not teach determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated. It has been held by the courts that to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. See, *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). As the Examiner states, neither Tammemae nor Chang, taking singly or in combination, teach or suggest all of the features of independent claim 11.

The Examiner contends that Raimi et al., U.S. Patent No. 5,604,895 (hereinafter "Raimi"), teaches the steps of reading in the source code line by line while effecting syntax analysis, and also determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated, and that it would have been obvious to one of ordinary skill in the art to modify the combination of Tammemae and Chang with Raimi.

Raimi addresses the problem of how to evaluate the simulation test coverage of an electrical circuit (column 1, lines 18-19) and teaches a method and data processor to estimate the simulation test coverage that a suite of simulation input programs provides for a given HDL model on an electrical circuit (column 3, lines 31-33). Thus Raimi's invention is directed to evaluation of an electrical circuit, not of a bus. With respect to a bus, Raimi discloses that "A bus is coupled to the memory unit. A central processing unit (CPU) is coupled to the bus to allow communication between the CPU and the memory unit" (column 2, lines 38-40), and that, "FIG. 2 illustrates a central processing unit (CPU) 18 coupled to a memory unit 20 via a bus"

(column 15, lines 1-2). Further, Raimi discloses "Inside the memory unit 20, there is an original high level circuit description 21, which is a file, or set of files, containing a high level language, possibly HDL, description of an electrical circuit and there is a new high level language, possibly HDL, circuit description 22, which is a file, or set of files, containing a description of the same circuit as is modeled in the original high level language description 21 but with monitor code added to estimate test coverage." (column 15, lines 2-10). Accordingly, the bus taught by Raimi is simply the physical bus, known to those skilled in the art, used for the purpose of transmission of instructions and information between the CPU and memory.

Thus Raimi simply teaches the bus definition realizing the input/output operation of data with regard to the memory (20) because Raimi can perform evaluation or estimation of data sent via the bus for the purpose of the evaluation of the electrical circuit, but not for the purpose of optimization of the bus. Hence no description regarding the bus optimization is found in the specification. Therefore, the physical bus disclosed by Raimi is distinct from the virtual bus of the present invention.

The present invention is directed to a method for performing a performance evaluation on *at least one bus*. In terms of the design phase, the present invention is distinguishable from Raimi in the creation of the hardware/software architecture. Because Raimi discloses a method and apparatus for determining test coverage estimation for an electrical circuit, he uses a specific high level language description of an electrical circuit (column 15, lines 5-6). In contrast, the present invention uses source code describing an algorithm design in a general purpose high-level programming language, as recited in independent claim 1. Because the present invention performs a performance evaluation of a bus at a high-level stage of the design and development

process, both the hardware and software of the present invention are necessarily distinct from that of Raimi.

Moreover, because Raimi does not teach or suggest evaluating the performance of a bus, he does not teach determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto *the bus to be evaluated*, as recited in claim 11.

As illustrated above, neither Tammemae nor Chang nor Raimi, taking singly or in any combination, teach or suggest all features of independent claim 11. Accordingly, this independent claim is patentable over the art of record in the application. In addition, claims 12-15 and 17-19 depend from claim 11, incorporating all of the features and limitations of the base claim, so that these dependent claims are patentable over the prior art. Thus applicant requests that this rejection be withdrawn.

**Rejection of Claims 16 and 22 Under 35 U.S.C. §103**

Claims 16 and 22 are rejected under 35 U.S.C. § 103(a) as unpatentable over Tammemae in view of Chang and further in view of Raimi. This rejection should be withdrawn based on the comments and remarks herein.

As discussed above, the Examiner states that Tammemae and Chang do not expressly teach the sequentially reading, determining, modifying and repeating steps of claim 16, and that Raimi teaches these steps, and that it would have been obvious to one of ordinary skill in the art to modify the combination of Tammemae and Chang with Raimi.

As discussed above, Raimi does not disclose or suggest a virtual bus or evaluating the performance of a bus. Thus, Raimi does not teach or suggest determining whether the source

code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated as recited in independent claims 16 and 20.

Thus, as illustrated above, the hypothetical combination of Tammemae, Chang and Raimi does not disclose each and every limitation recited in claims 16 and 20. Claim 22 depends from claim 20, incorporating all of the features and limitations therein. Accordingly, the rejection of claims 16 and 22 should be withdrawn.

**Rejection of Claims 20-21 and 23-26 Under 35 U.S.C. §103**

Claims 20-21 and 23-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tammemae in view of Raimi. This rejection should be withdrawn based on the comments and remarks herein.

The Examiner contends that Raimi teaches determining whether a line of source code represents writing data onto the bus to be evaluated. However, Raimi only teaches storing whether each of the assignment statements has been executed (column 2, lines 54-55) but does not teach or suggest determining details about an assignment statement. Specifically, Raimi does not teach or suggest determining whether a line of source code represents writing onto the bus, as recited in independent claim 20. As discussed above, the bus disclosed by Raimi is simply the physical bus used for the purpose of transmitting instructions and information between the CPU and memory. No determinations about what is written to the bus are disclosed by Raimi.

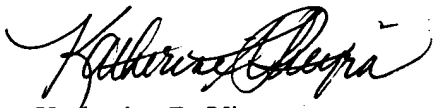
As illustrated above, the hypothetical combination of Tammemae and Raimi does not teach or suggest all of the features of independent claim 20. Accordingly, this independent claim is patentable over the art of record in the application. In addition, claims 21 and 24-26 depend

from claim 20, incorporating all of the features and limitations of their base claim, so that these dependent claims are patentable over the art or record in the application. Accordingly, applicant requests that this rejection be withdrawn.

## CONCLUSION

For at least the reasons set forth in the foregoing discussion, Applicant believes that the application is now allowable and respectfully requests that the Examiner reconsider the rejections and allow the application. Should the Examiner have any questions regarding this Amendment, or regarding the Application generally, the Examiner is invited to telephone the undersigned attorney.

Respectfully submitted,



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